

A Scalable 6-to-18GHz Concurrent Dual-Band Quad-Beam Phased-Array Receiver in CMOS

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Outline

➤ Introduction

- Proposed Concurrent Phased-Array System
- 6-to-18GHz Phased-Array Receiver
- Test Setups and Experimental Results
- Conclusion

Wideband Large-Scale Phased Arrays



Military radars

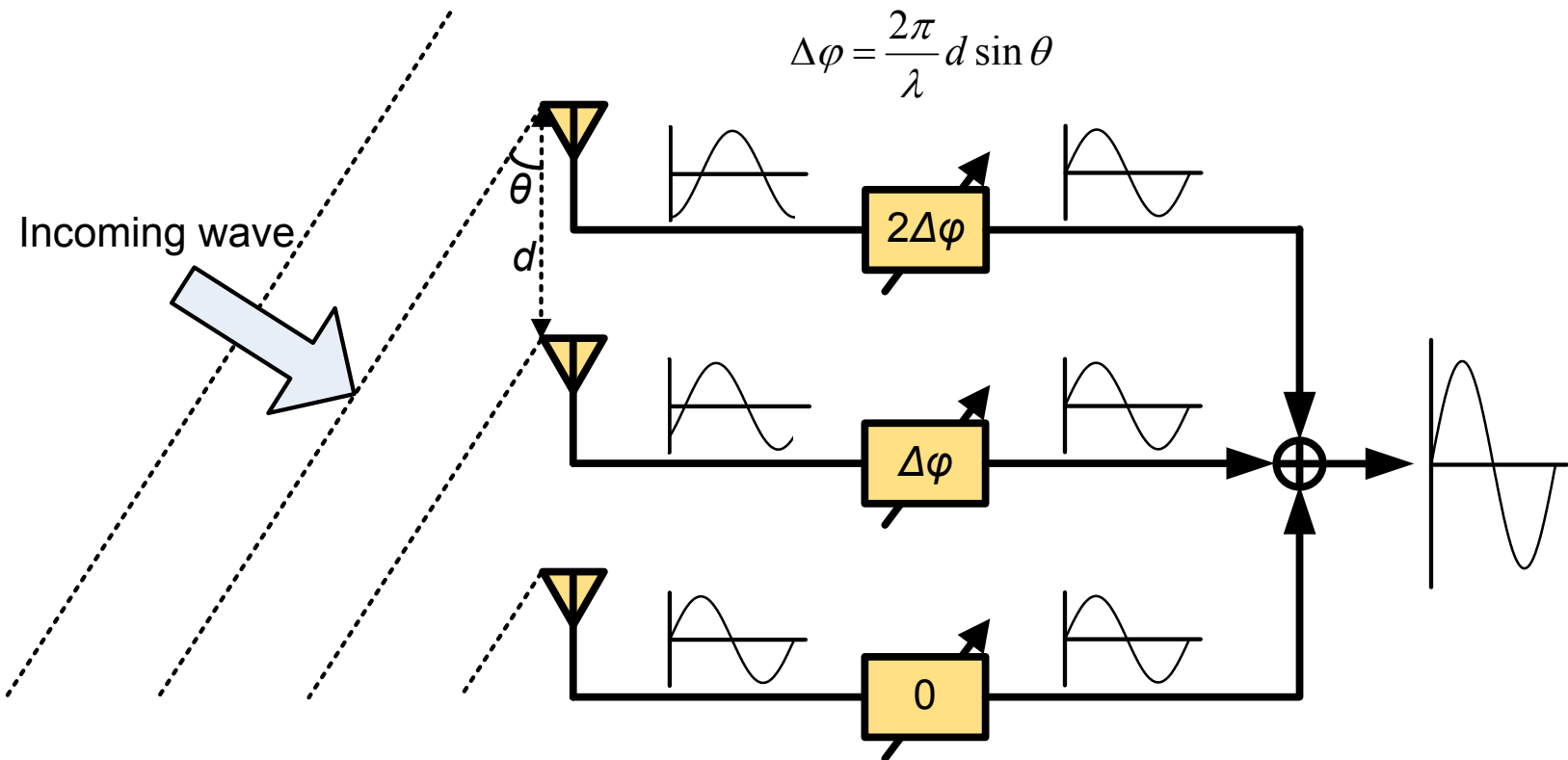


Space & satellite communications



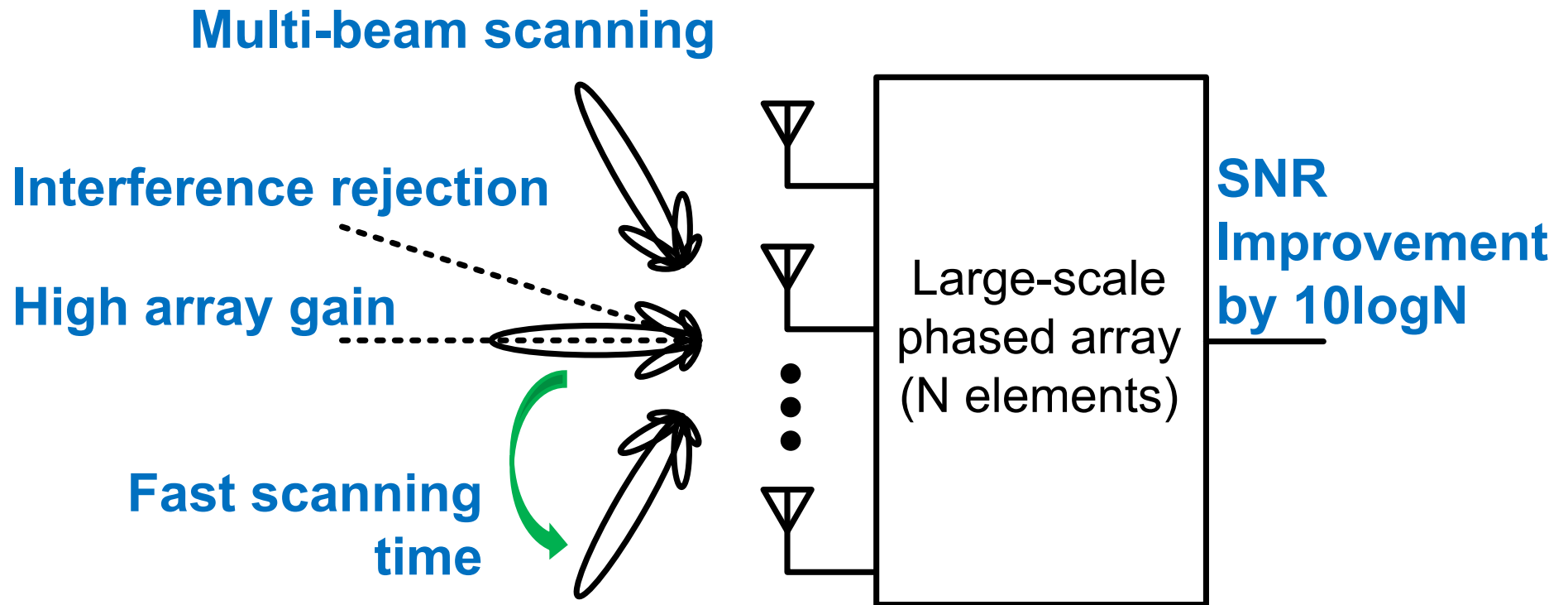
Weather radars

Phased Arrays

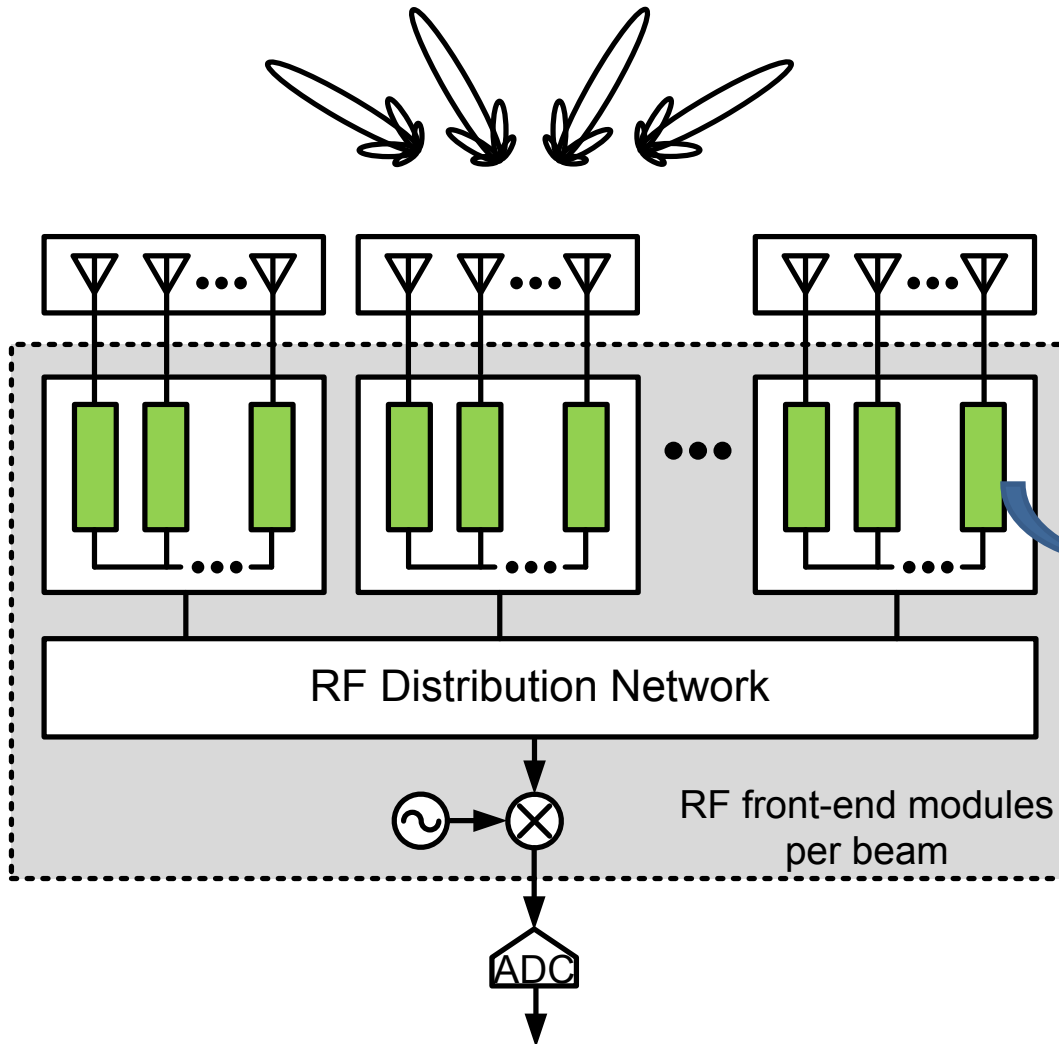


- Coherent addition of signals from each element.
- Reject other signals with different incident angles.

Advantages of Phased Arrays



Conventional Structure of Large-Scale Arrays



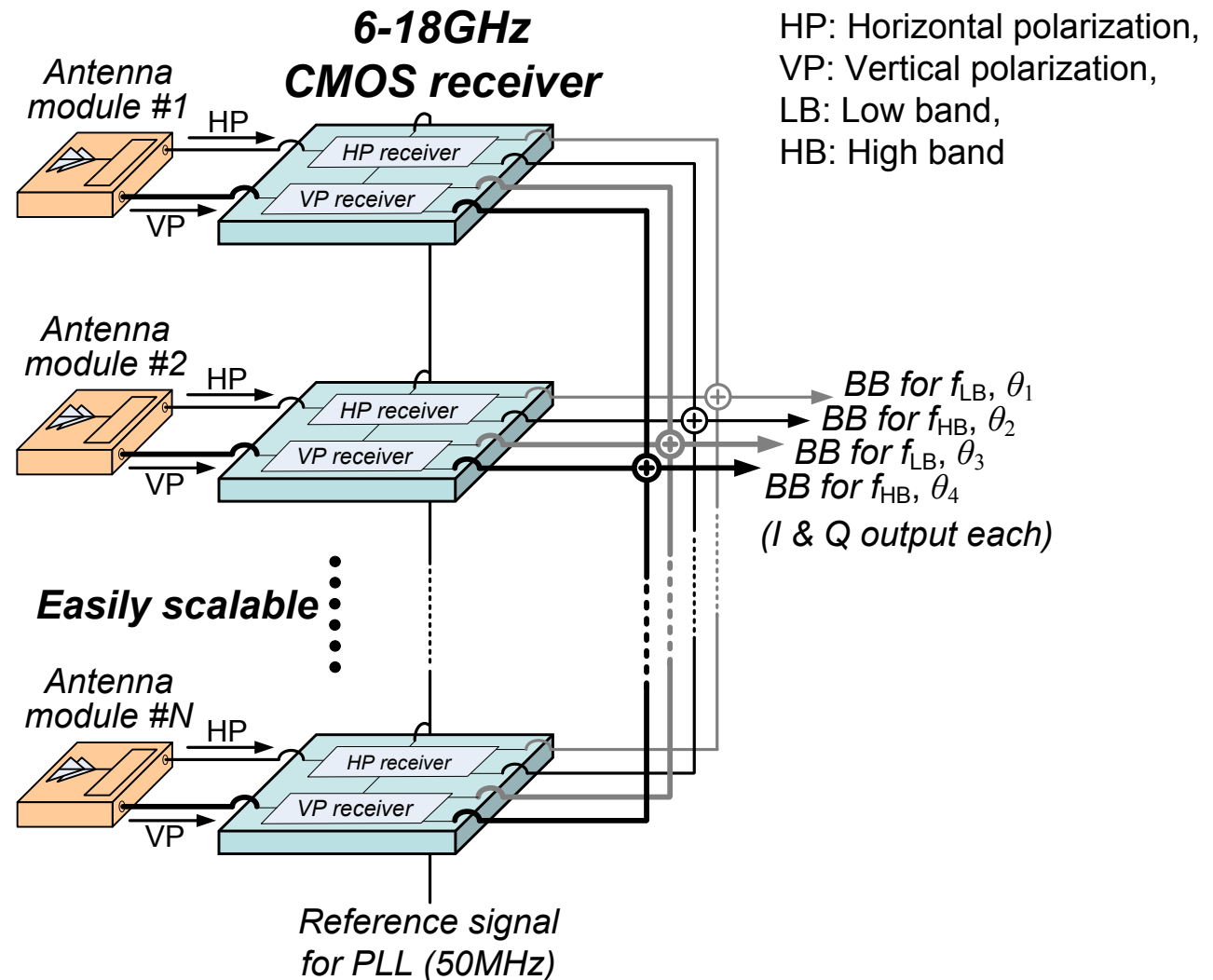
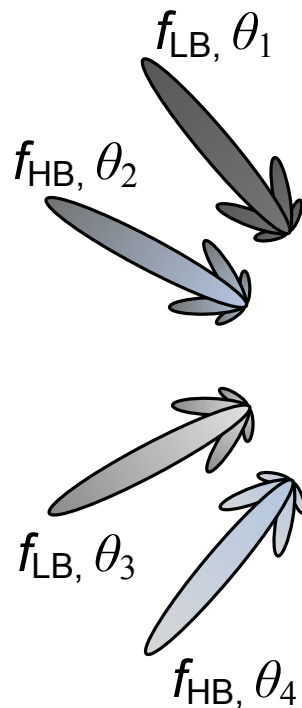
- Interconnection of separate modules.
 - Compound-semiconductor MMICs.
- ➡ High cost and complexity

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Tunable Concurrent Multi-Beam Array

Concurrent dual-band quad-beam receiving

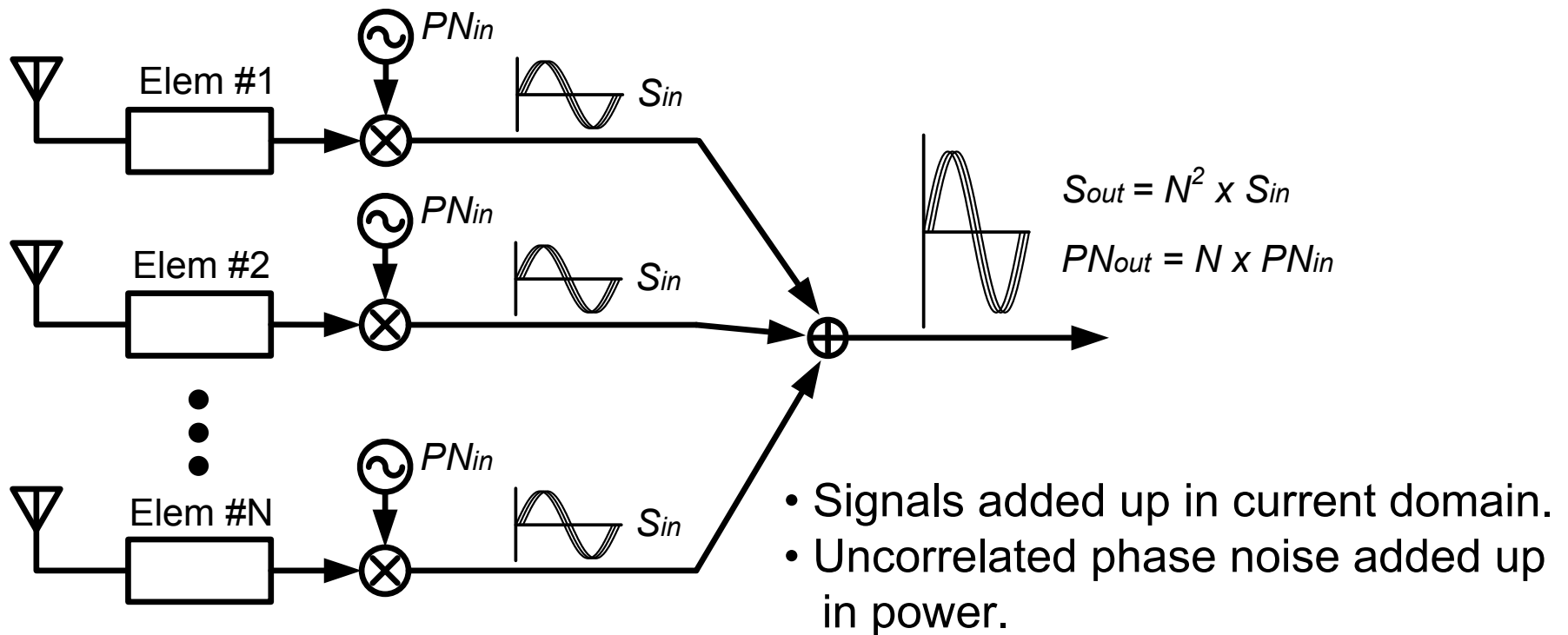


- Required components reduced dramatically.

Features of Proposed Concurrent Array

- Easily scalable to build large-scale arrays.
 - Dramatically reduce number of components required.
 - Low cost, low complexity, more reliability.
- Wideband operation (6 – 18GHz)
- Concurrent dual-band quad-beam scanning.
 - LB (6 – 10.4GHz) and HB (10.4 – 18GHz)
 - Two polarizations.
- Phase noise improvement in large-scale arrays.

Phase Noise Improvement



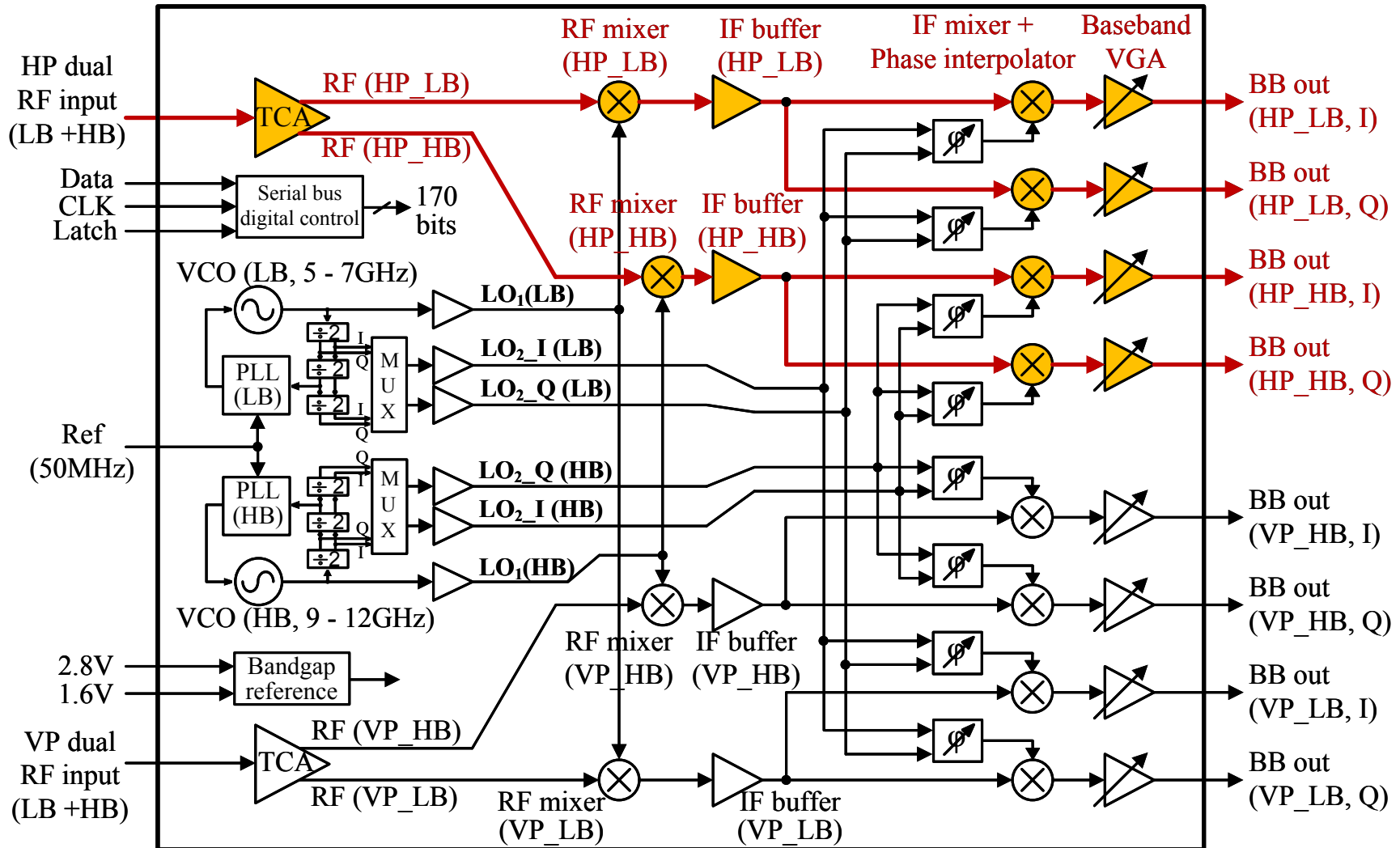
- Phase noise improved by $10\log_{10}N$.
- On-chip frequency synthesizers acceptable for the phase noise requirement.

Outline

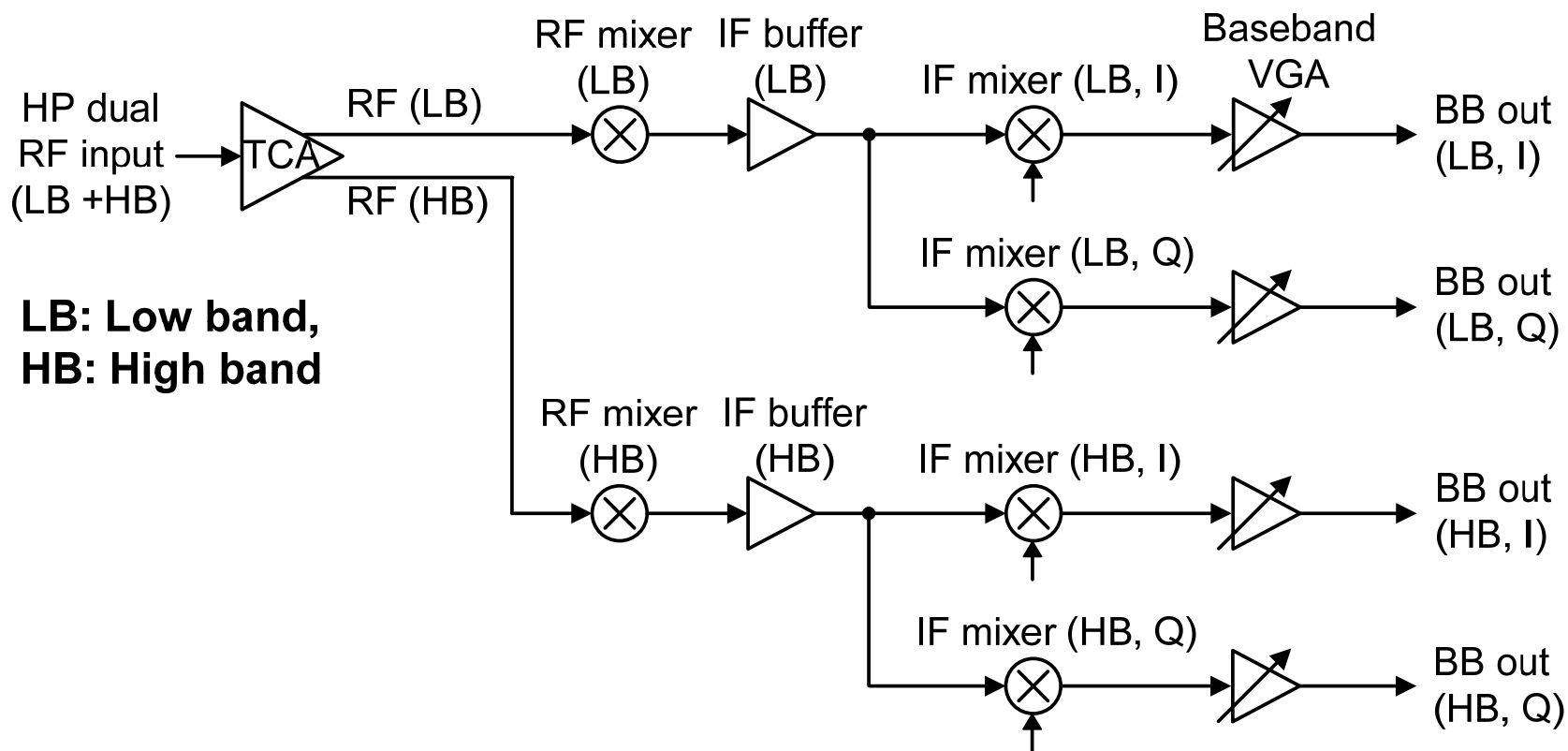
- Introduction
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Receiver Architecture

HP: Horizontal polarization, VP: Vertical polarization, LB: Low band, HB: High band

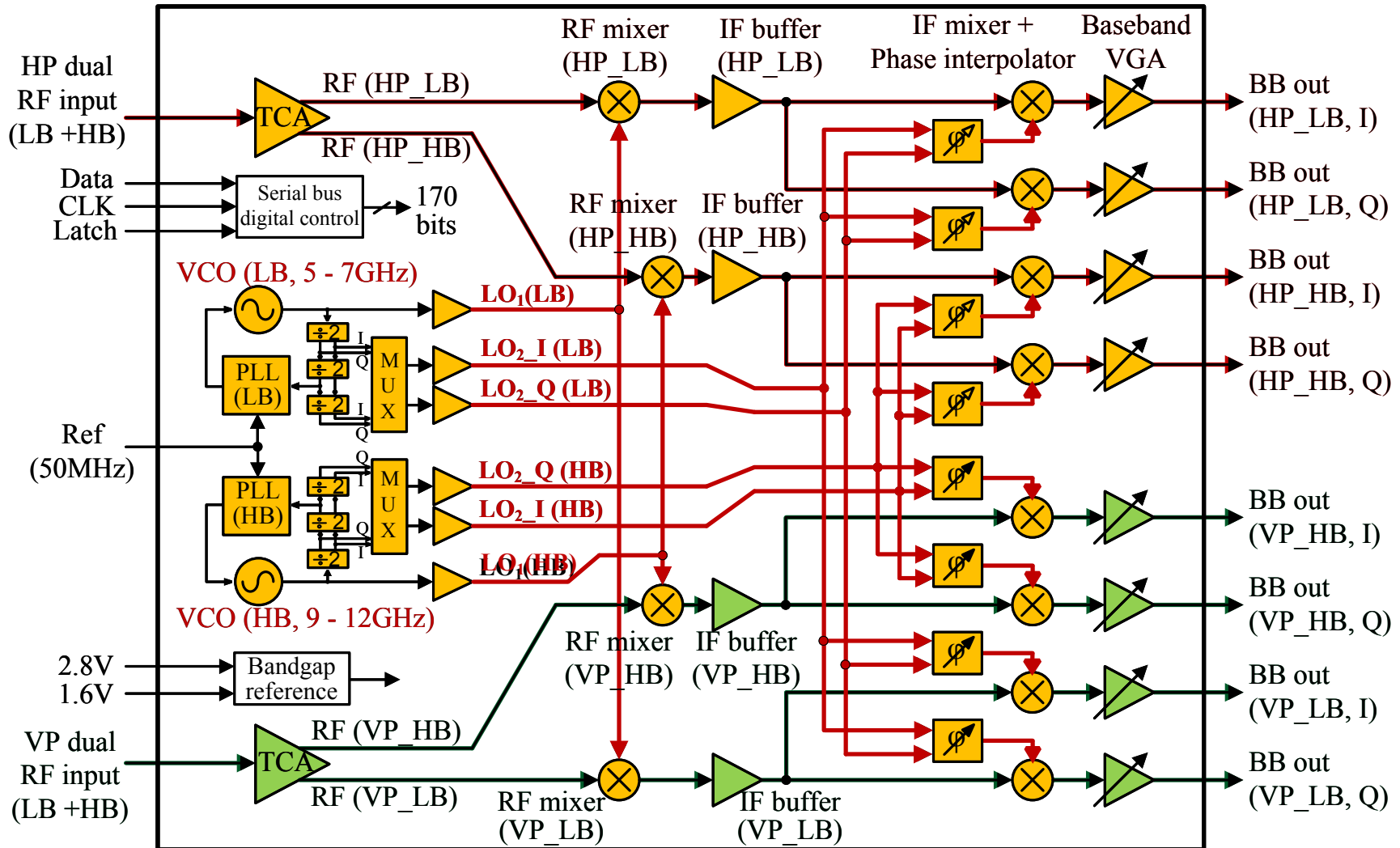


Receiver Architecture

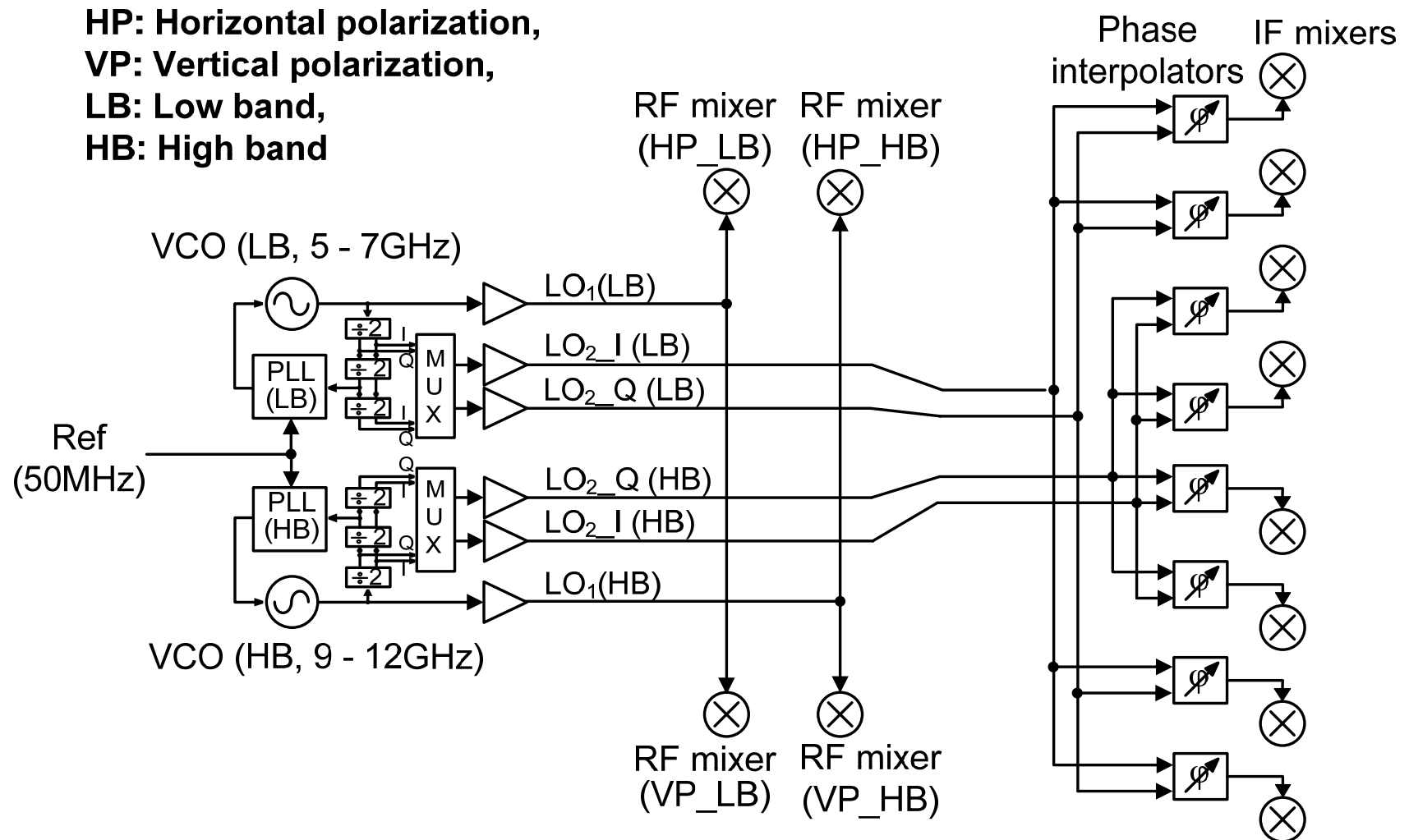


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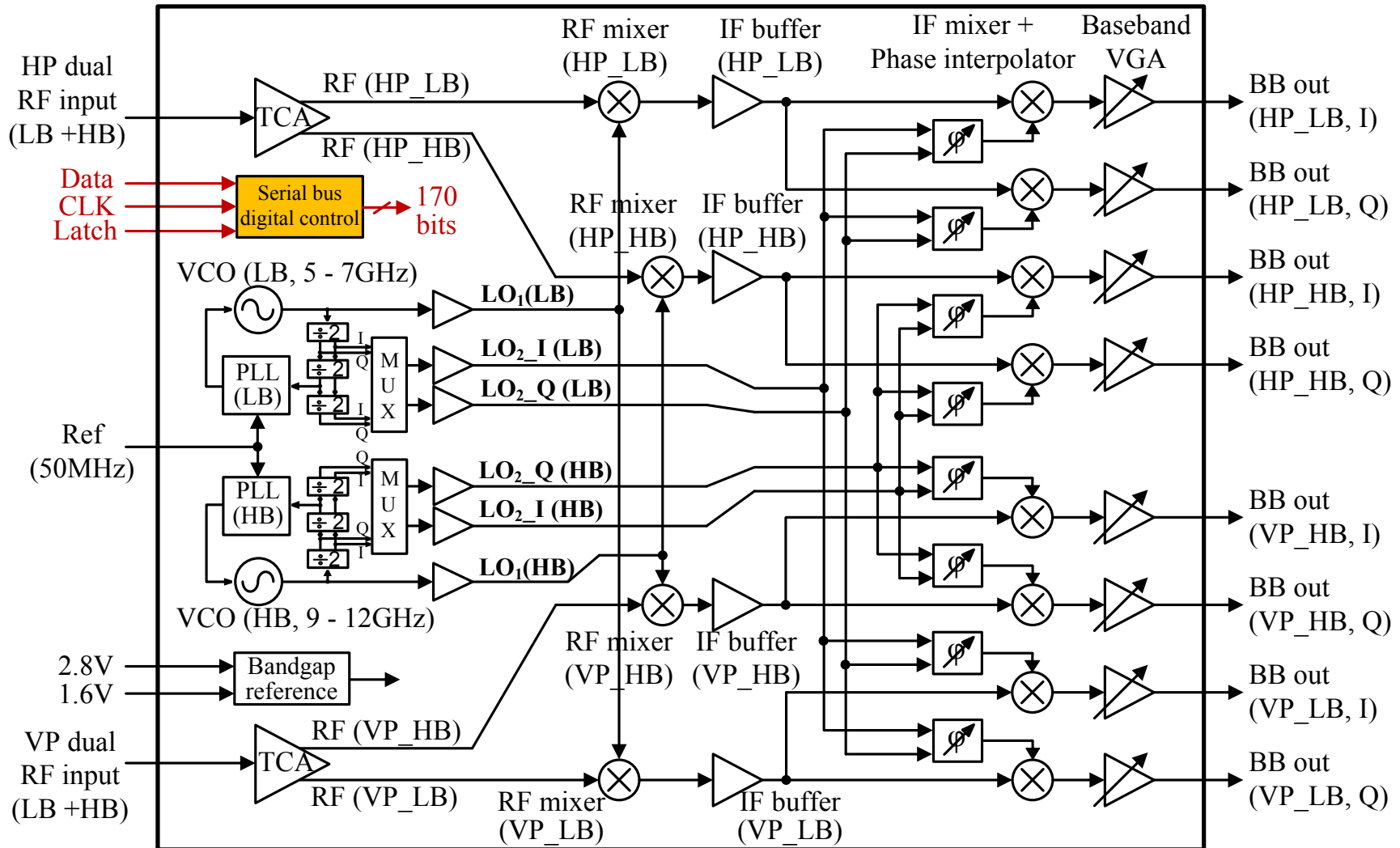


Receiver Architecture

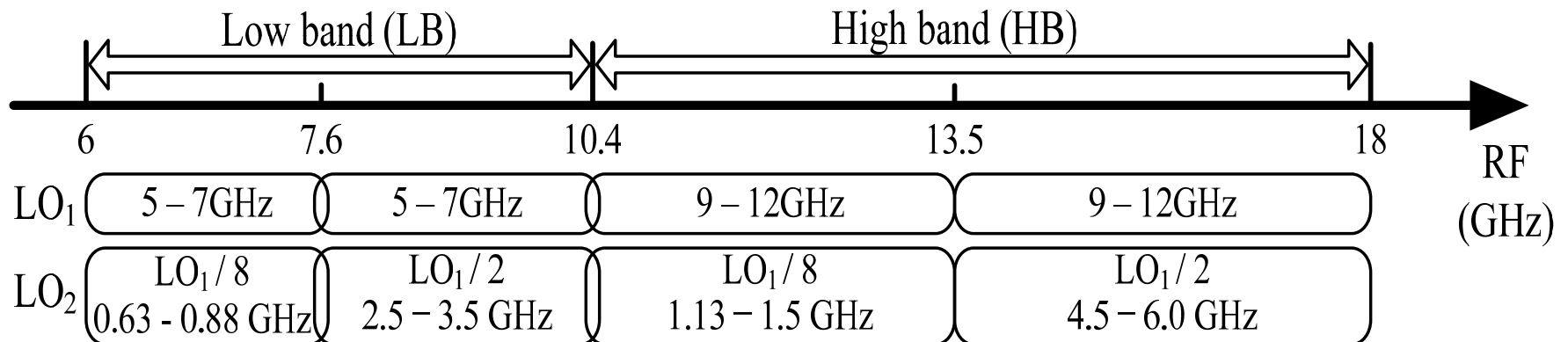


Receiver Architecture

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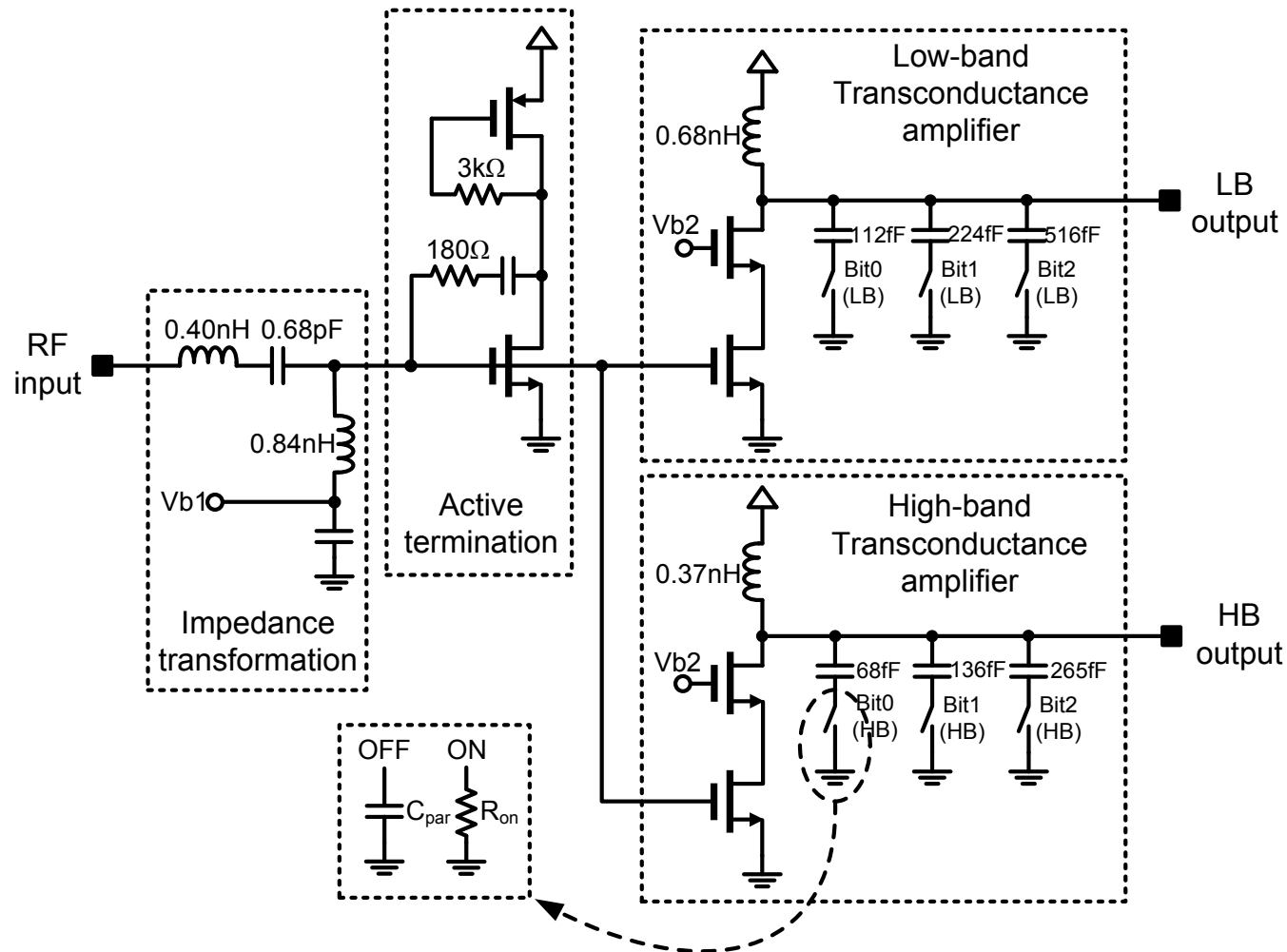


Frequency Plan



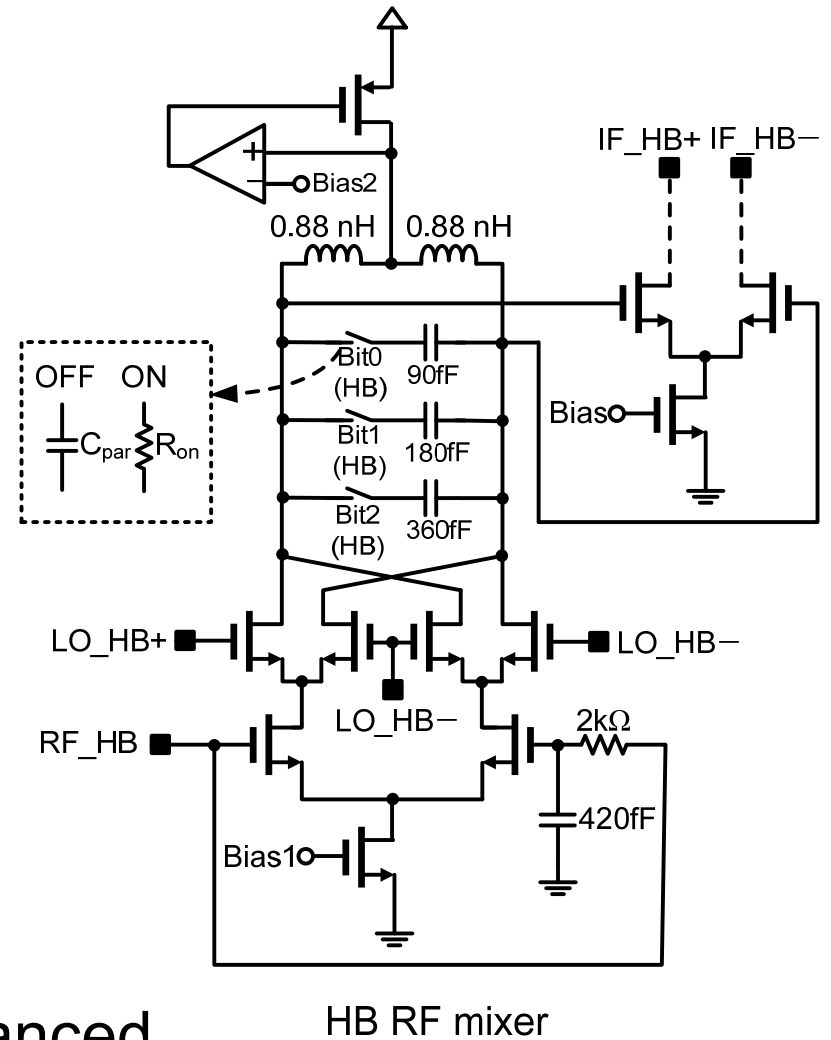
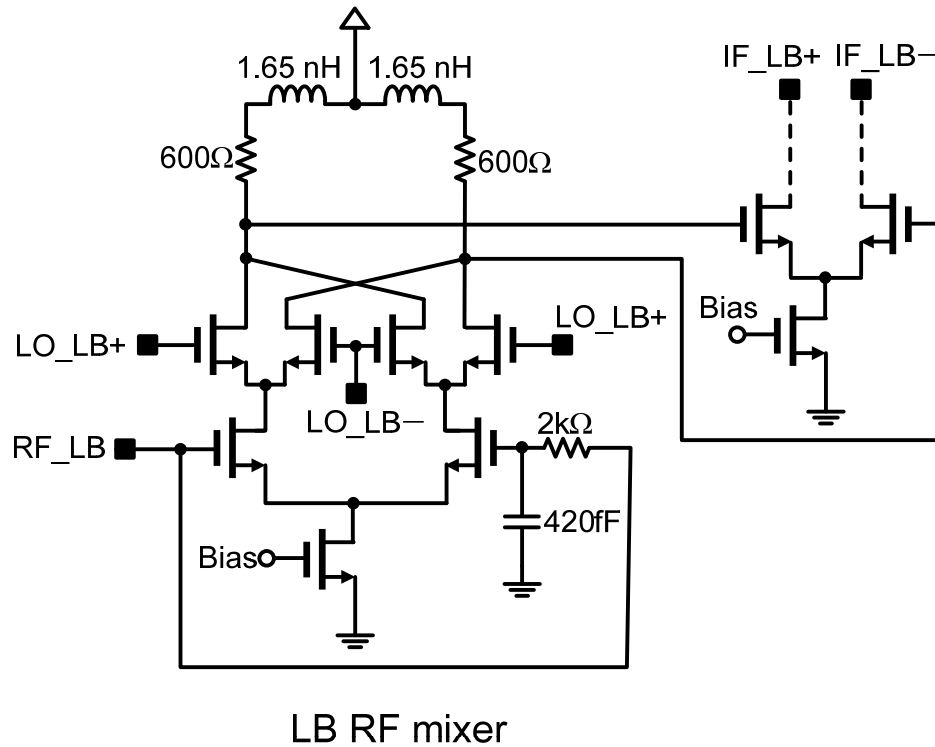
- LO₂ switches between 1/2 and 1/8 of LO₁, depending on IF frequency.
 - Performed by on-chip multiplexers.
 - Relax the required VCO tuning range.

Tunable Concurrent Amplifier (TCA)



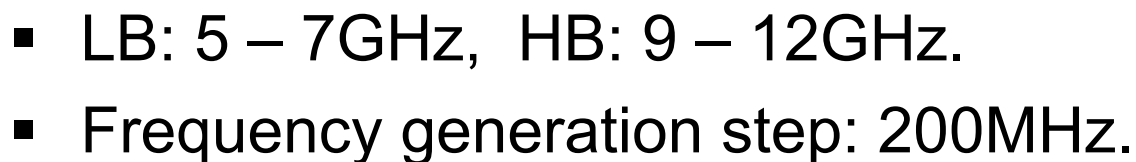
- Single-input, dual-output.
- Tunable LC loads for two separate tuned amplifiers.

Mixers

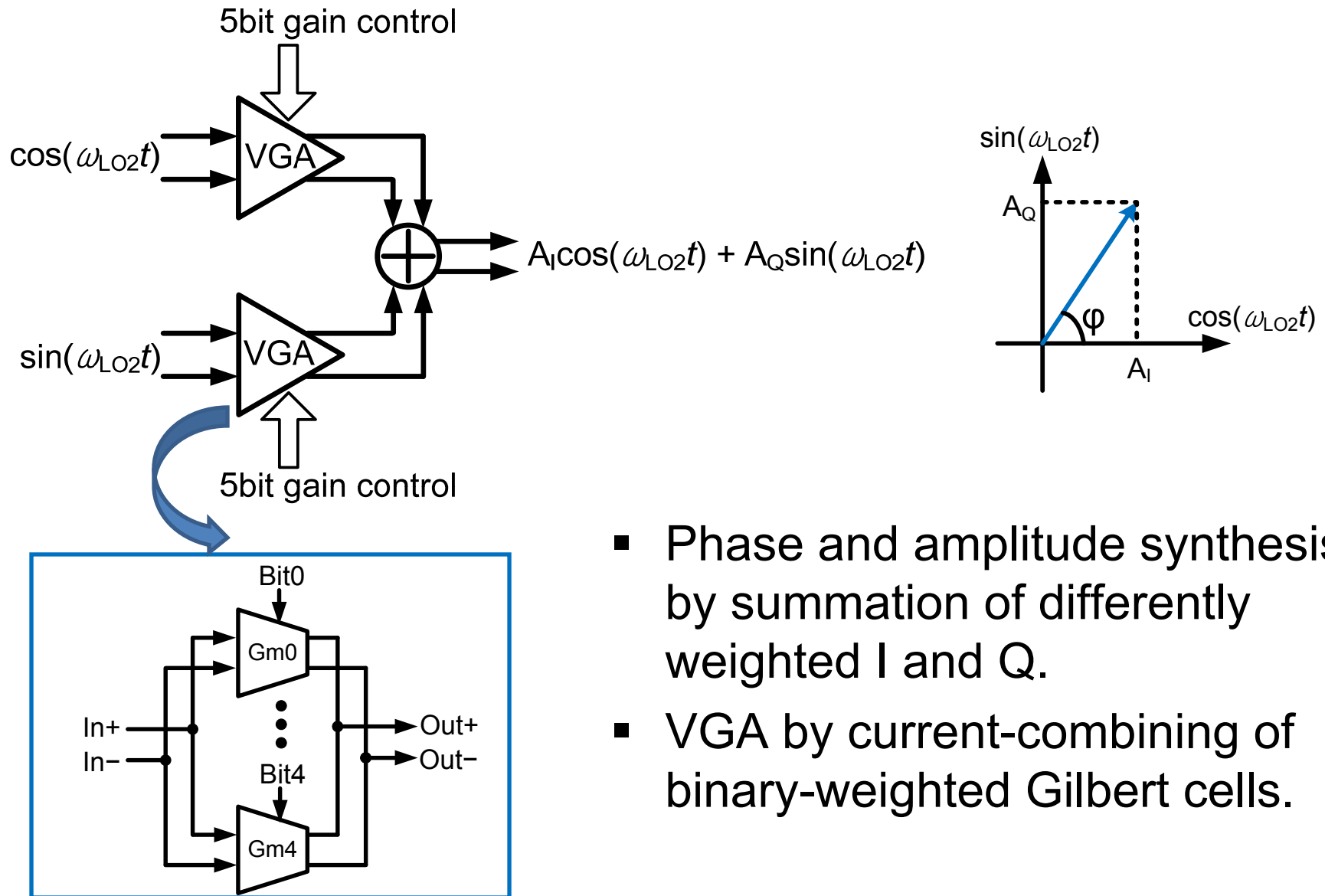


- Current commuting double-balanced mixers.

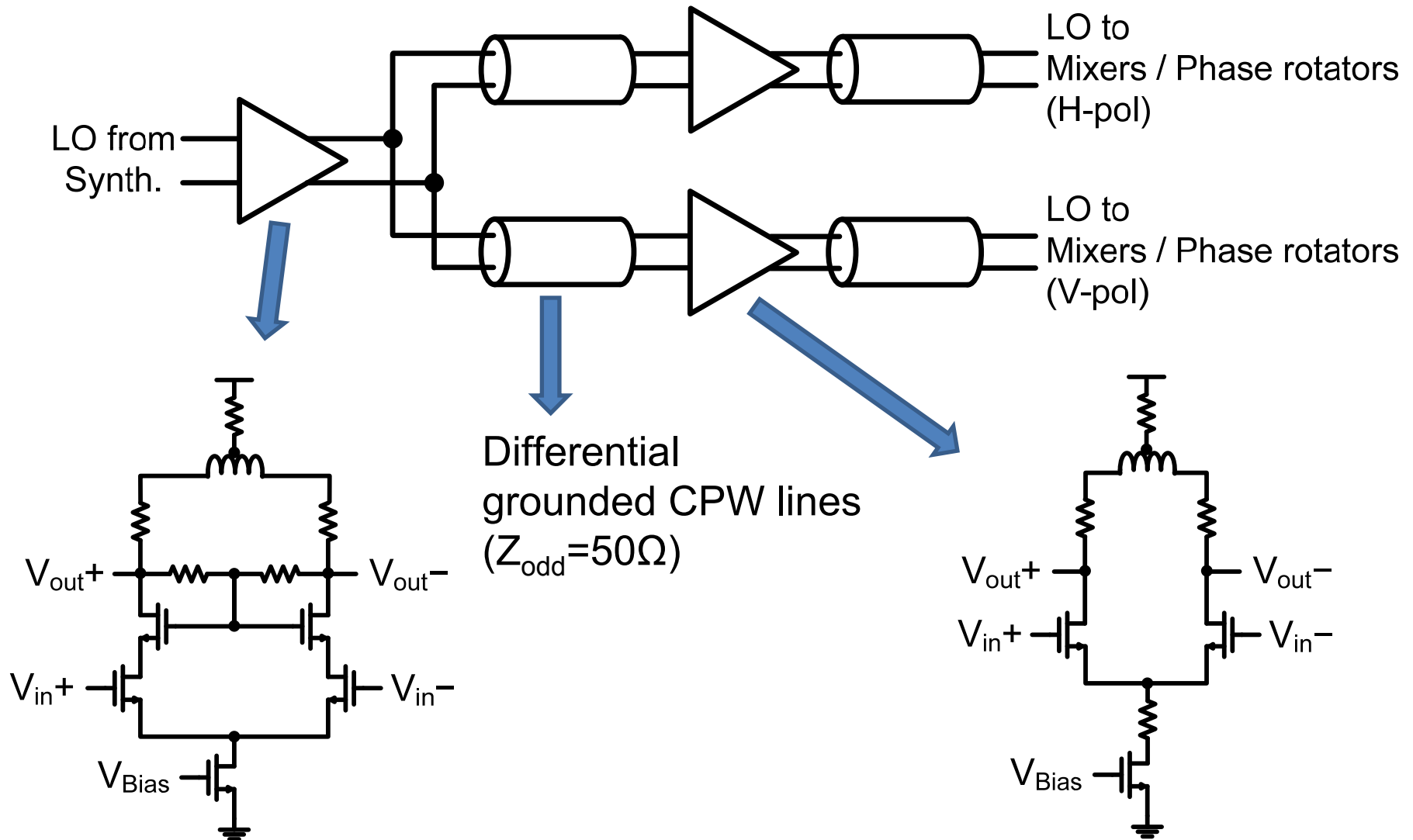
Architecture



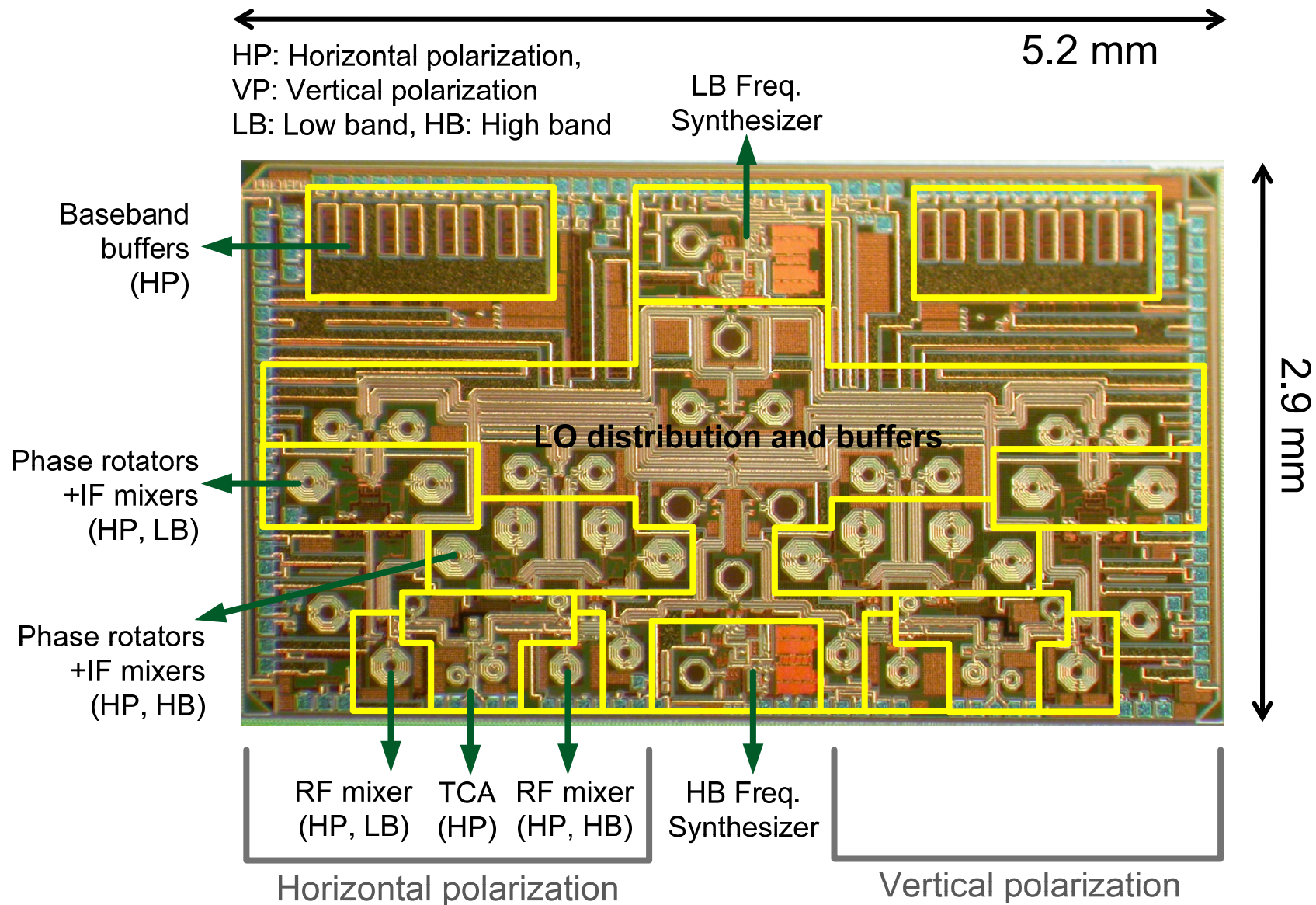
Digital Phase Rotators



LO Distribution and Buffers



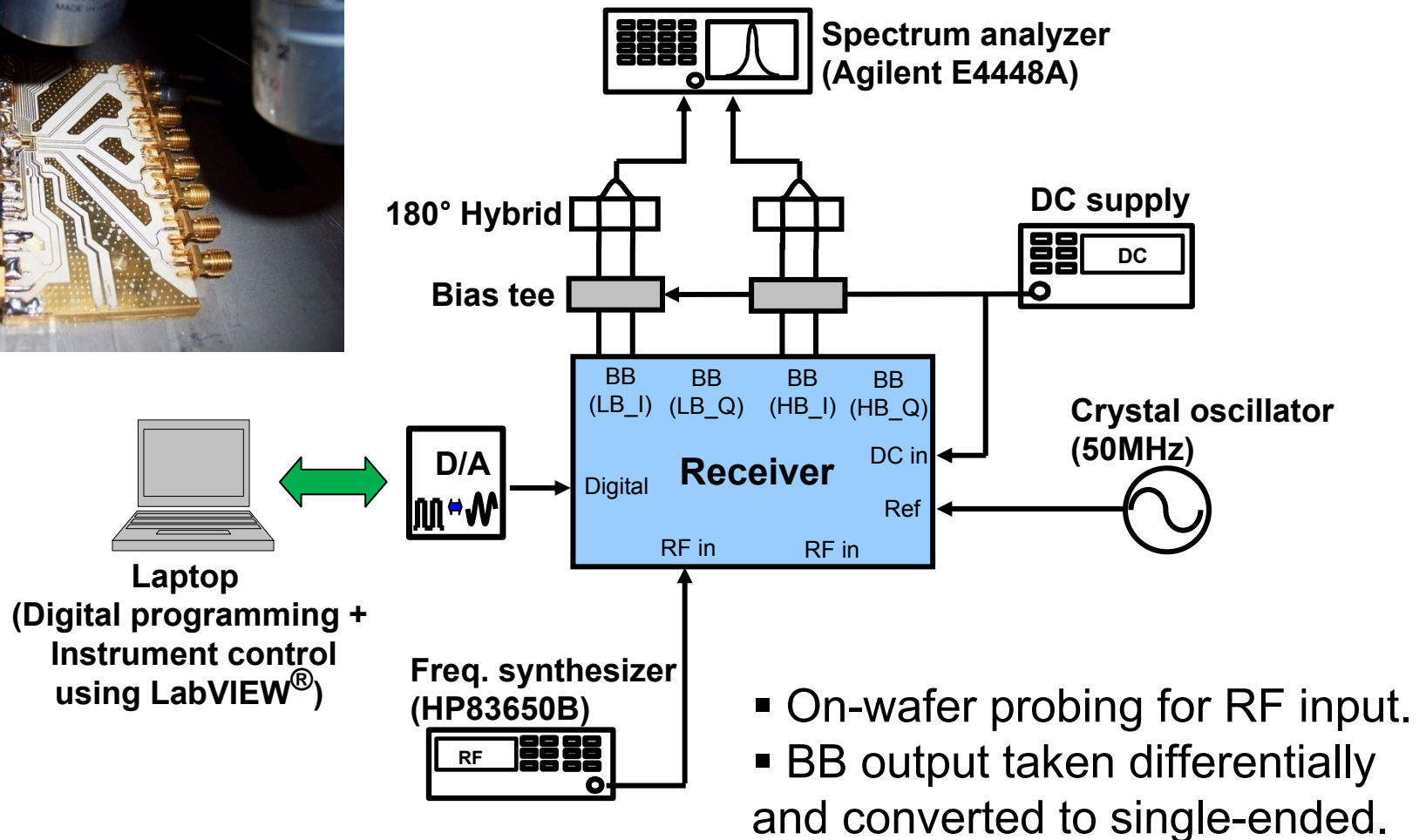
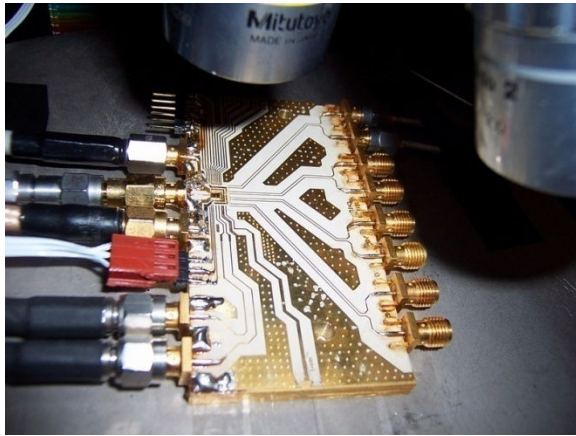
Chip Photograph



Outline

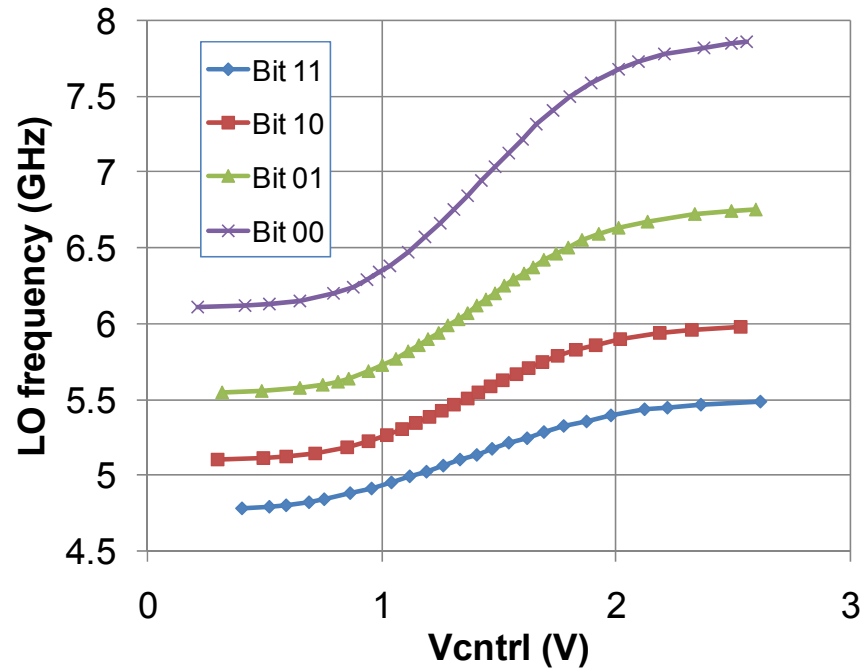
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Test Setup for Receiver Element



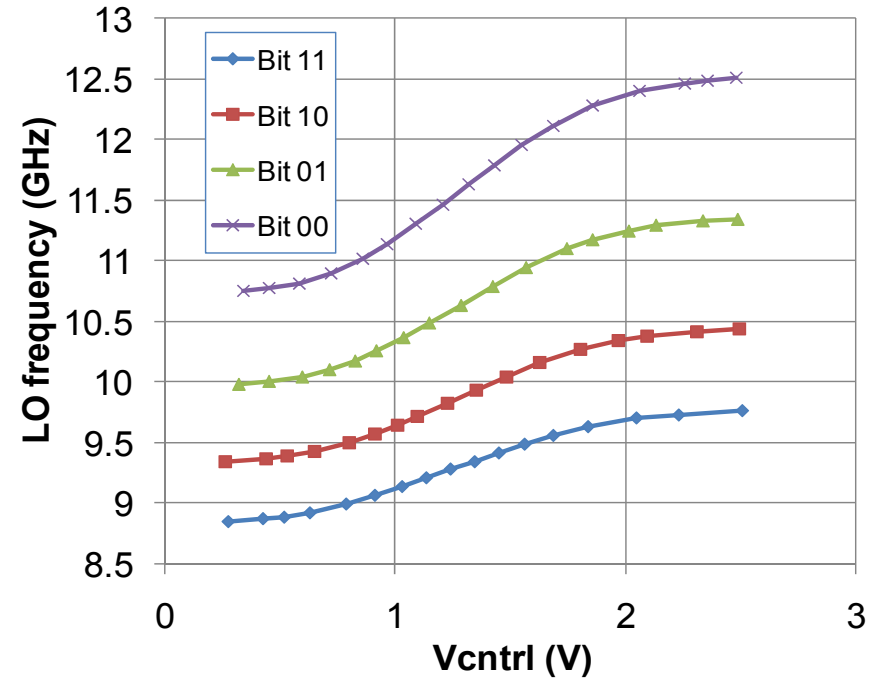
LO Generation

Synthesizer Locking Range (Low band)



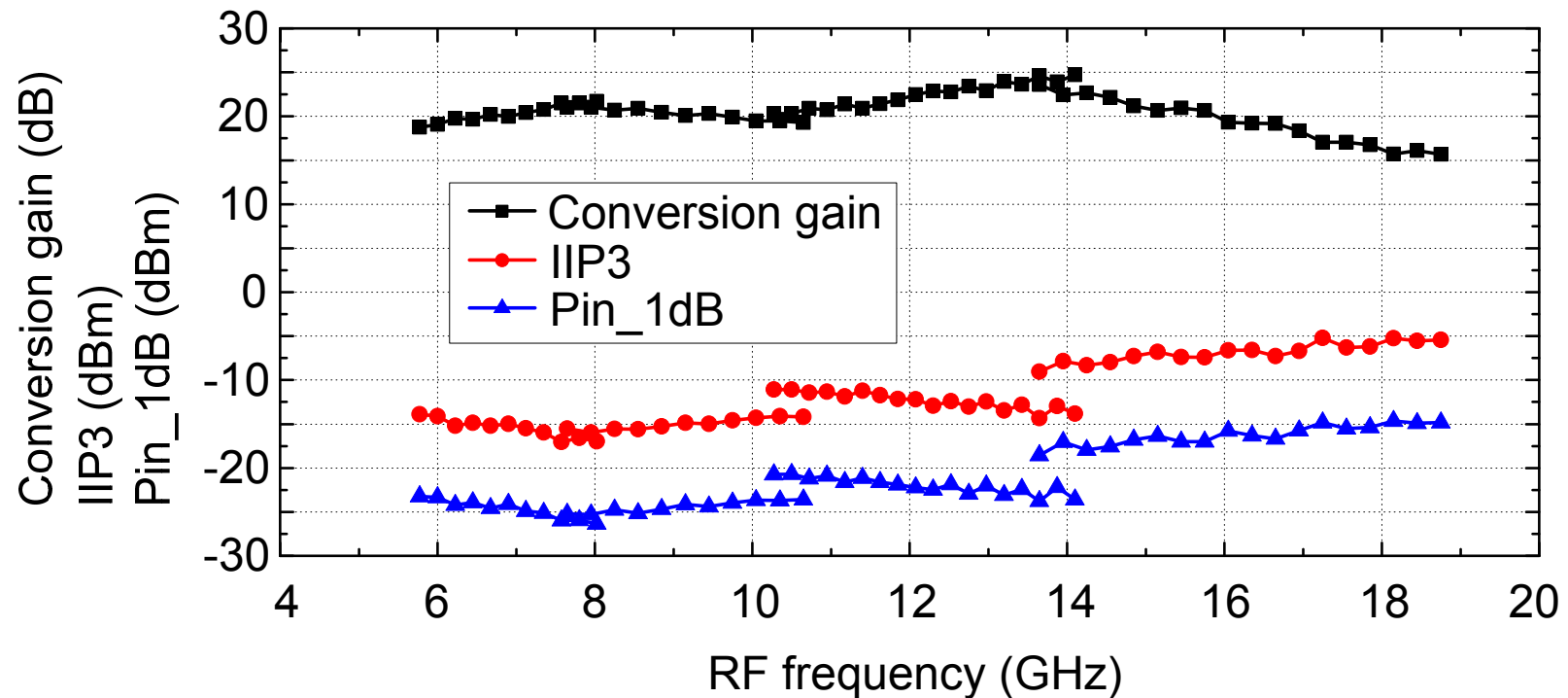
- Locking range:
4.8 – 7.8GHz

Synthesizer Locking Range (High band)



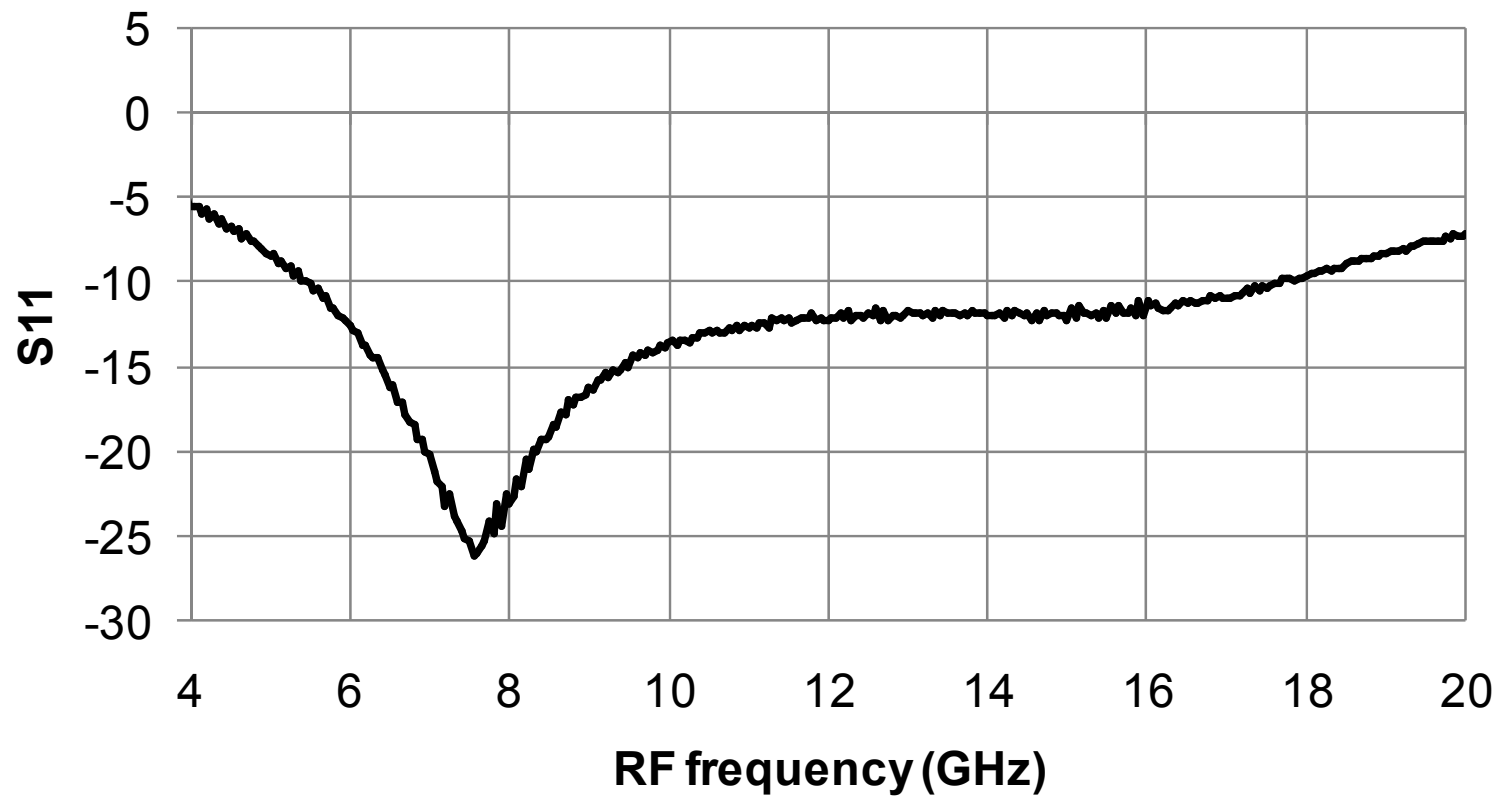
- Locking range:
8.8 – 12.5GHz

RF Performance



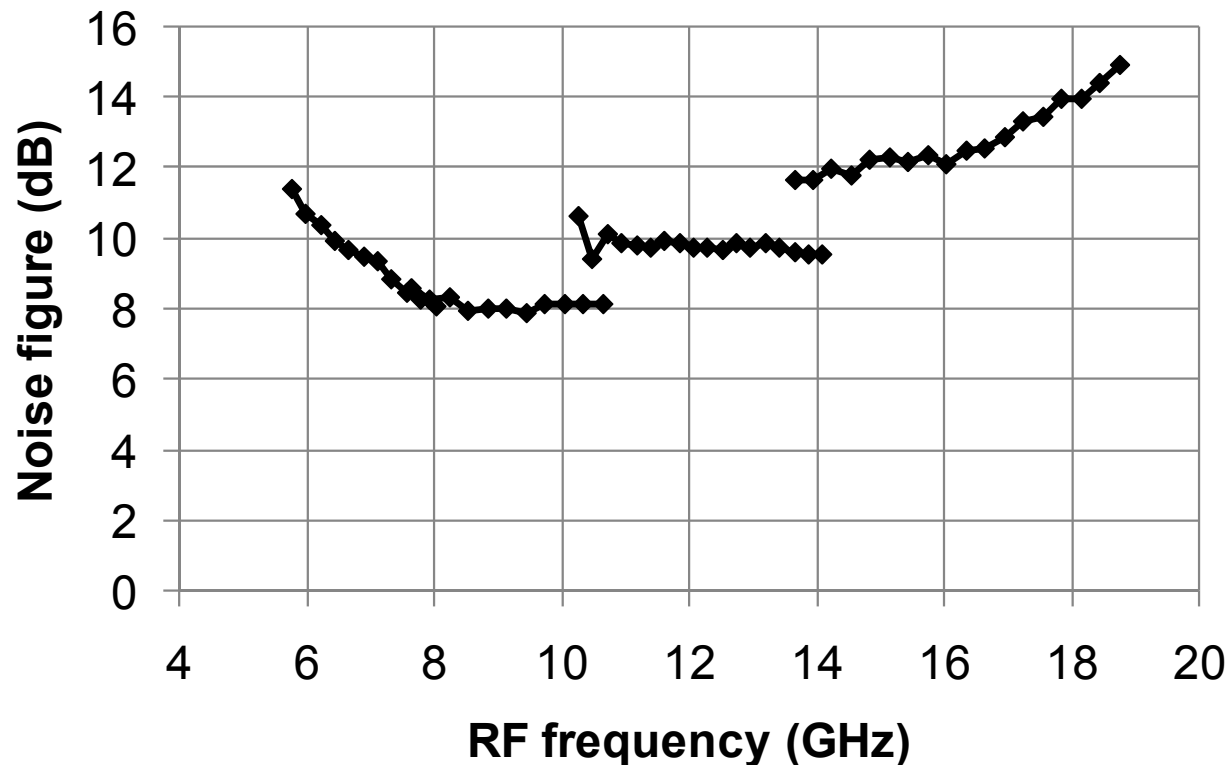
- Conversion gain = 16 ~ 24dB
- Pin_1dB = -25 ~ -15dBm
- IIP3 = -17 ~ -5dBm
- Discontinuities due to frequency band or scheme changes.

RF Input Matching



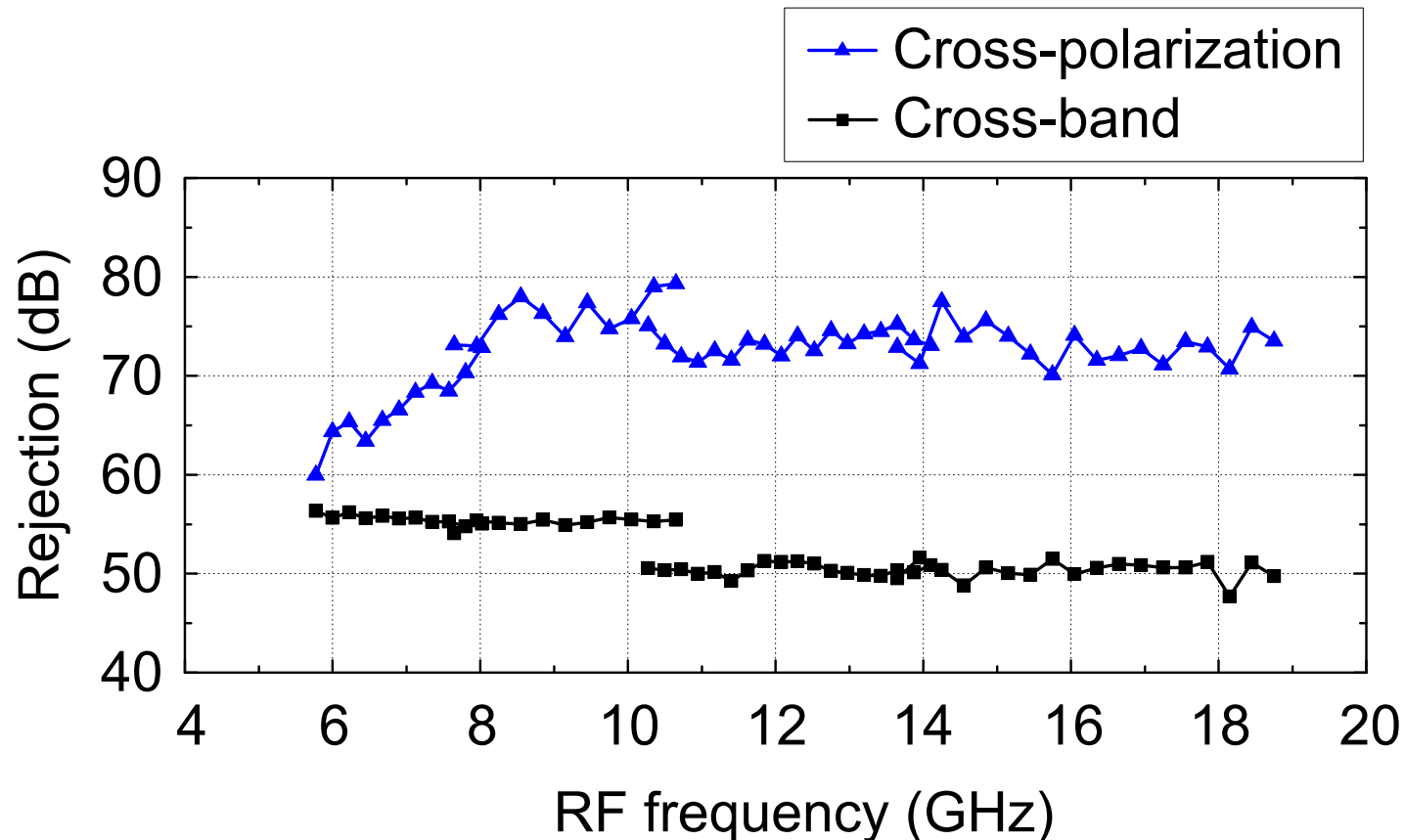
- Input matching insensitive to different TCA settings.

Noise Figure



- NF = 8 ~ 14dB across the entire band.
- 2.6 ~ 3.1dB, considering the preceding wideband GaN LNA in the active antenna module (2.5dB NF, 20dB Gain).

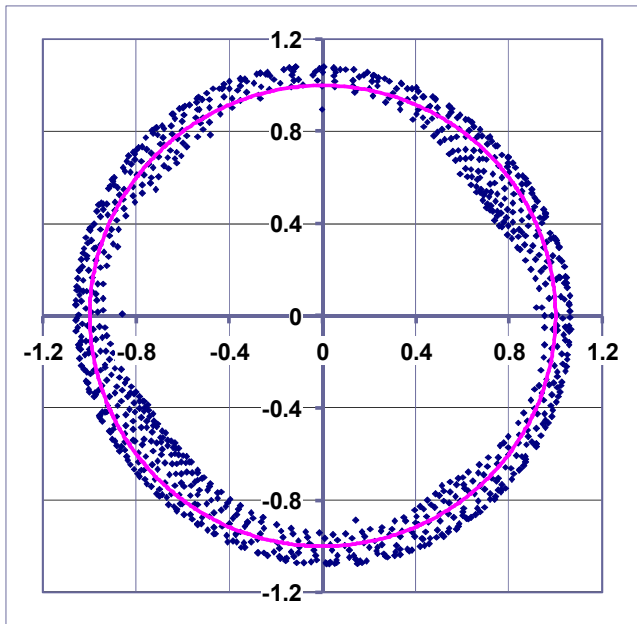
Isolation Performance



- Good isolations between two bands (more than 48dB) and between two polarizations (more than 62dB).

Phase Interpolation Performance

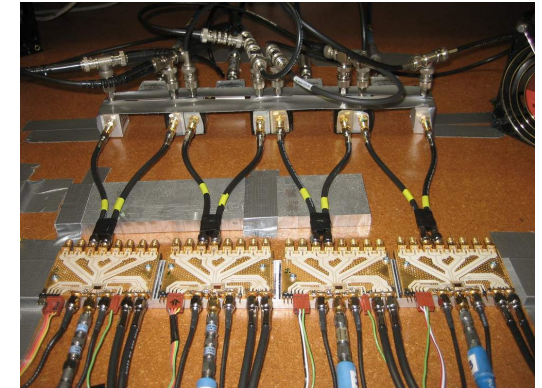
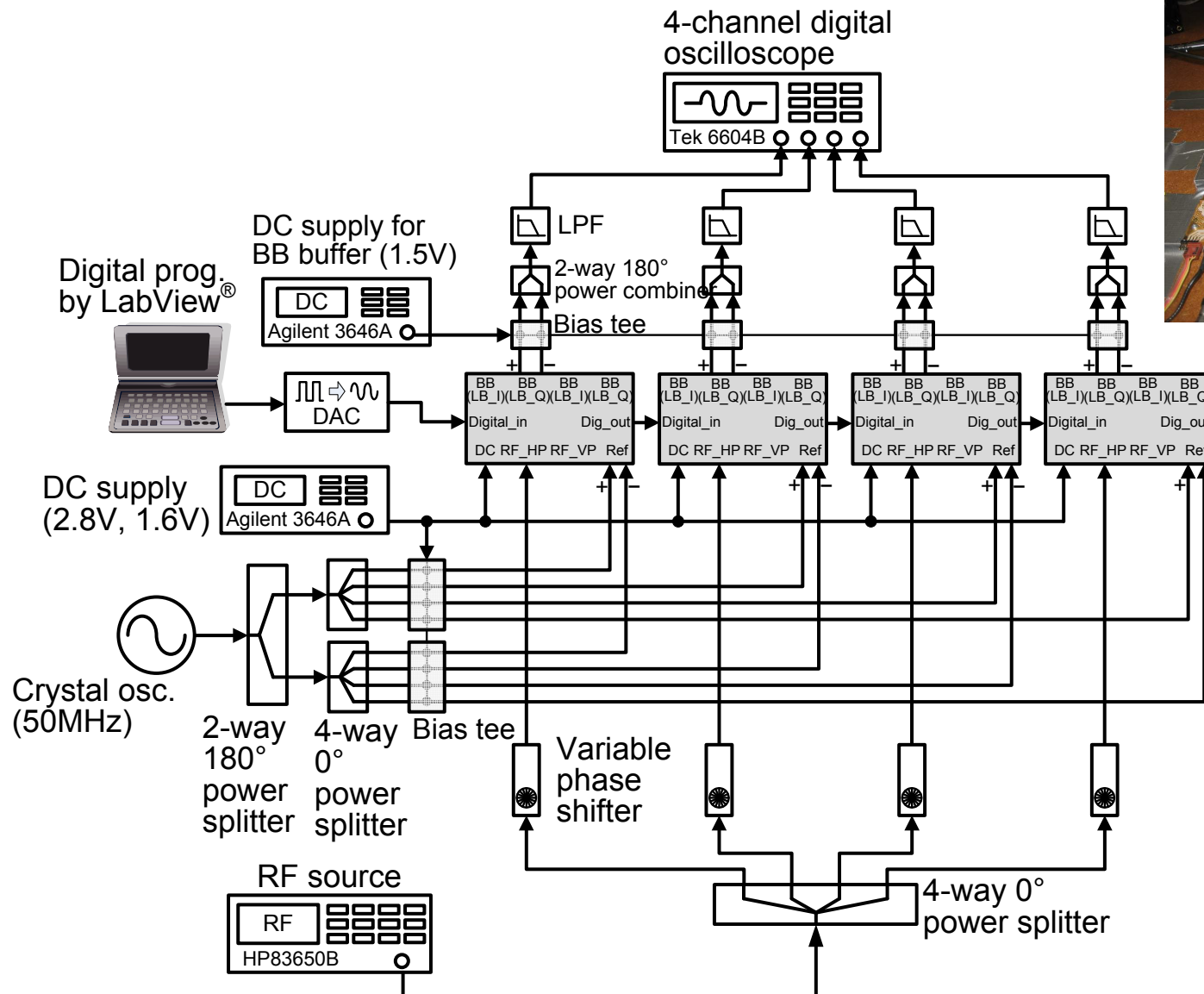
Measured constellation of interpolated baseband signal @18GHz



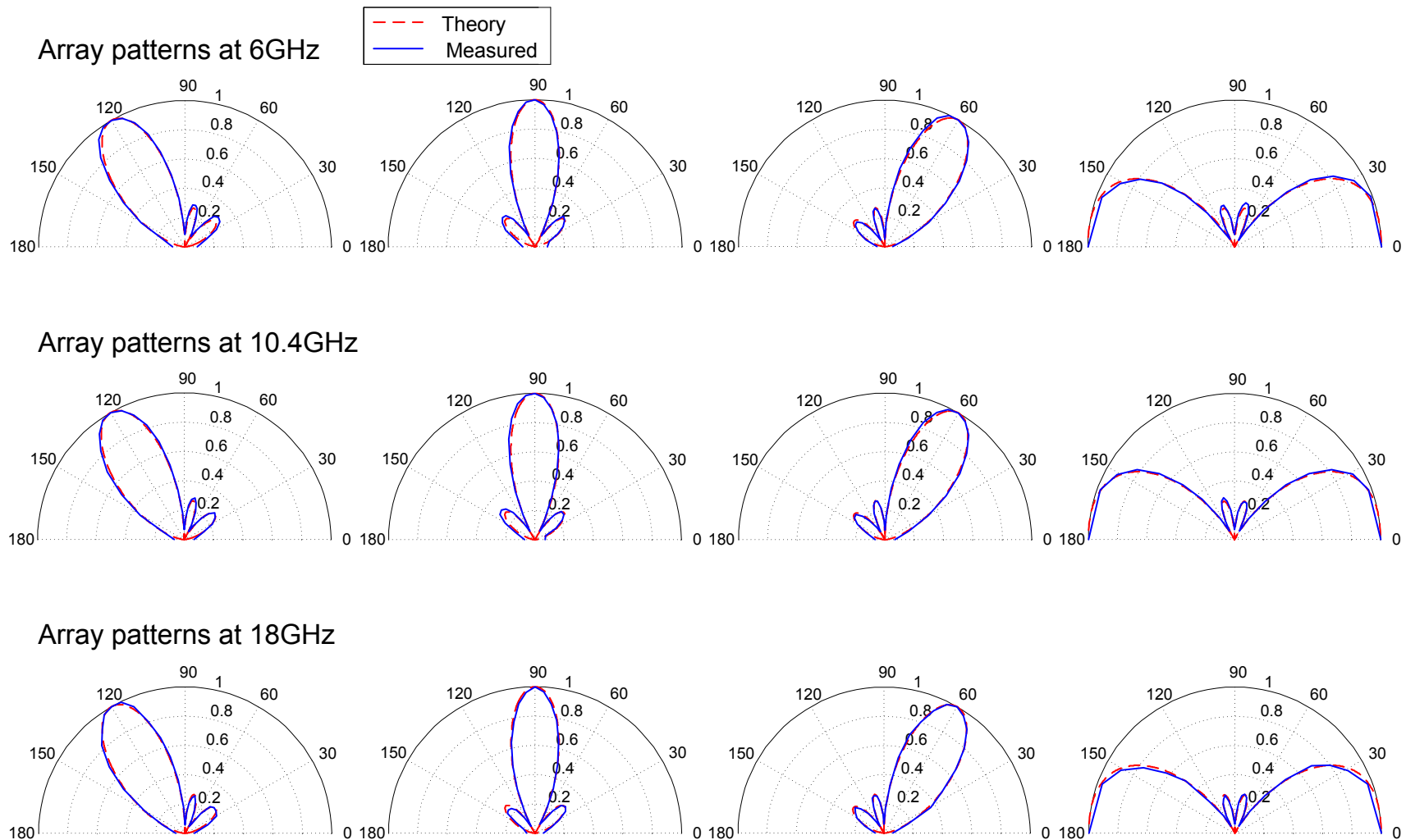
Phase interpolation performance summary

RF Freq.	Phase Error RMS	Phase Error Max.	Amp. Variation RMS	Amp. Variation Max.
6GHz	0.5°	2.6°	0.4dB	1.9dB
10.4GHz	0.2°	1.2°	0.2dB	1.5dB
14GHz	0.3°	1.4°	0.2dB	1.7dB
18GHz	0.2°	1.3°	0.5dB	2.3dB

Array Test Setup

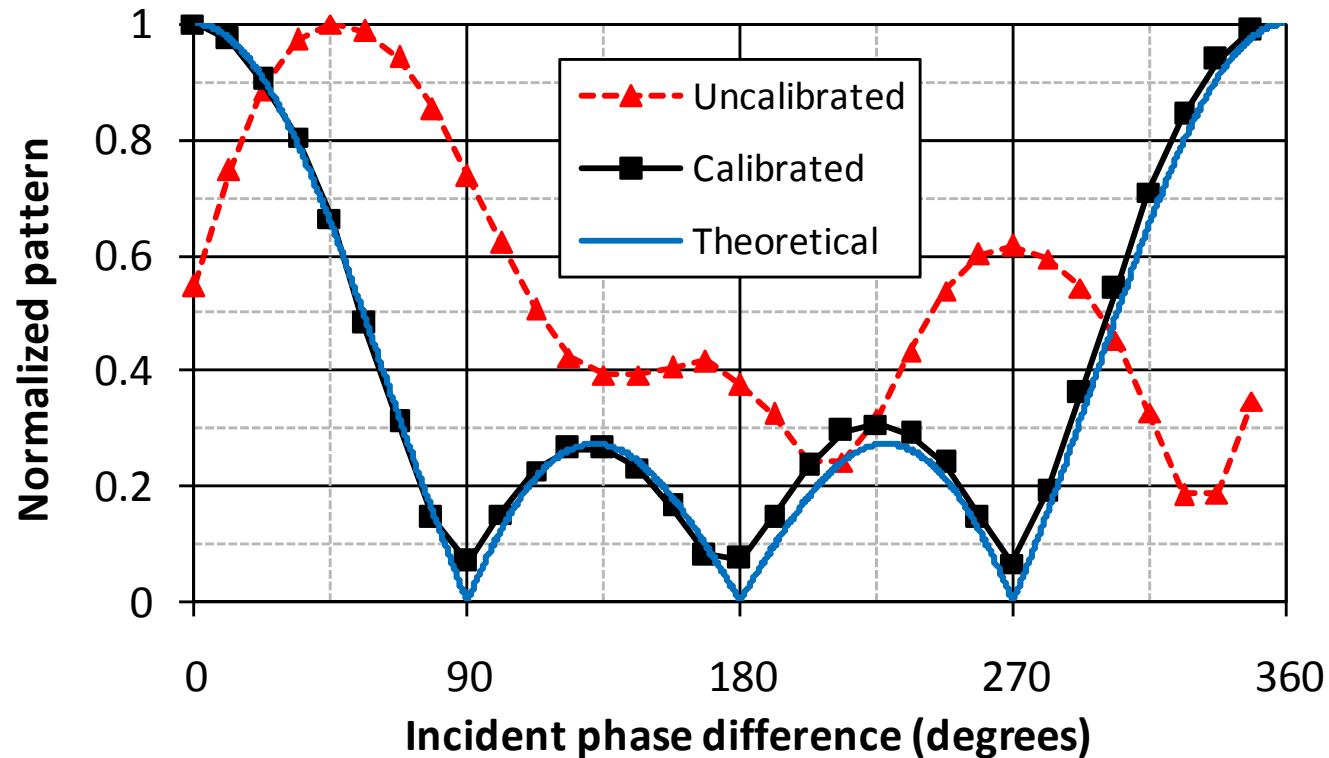


Array Patterns



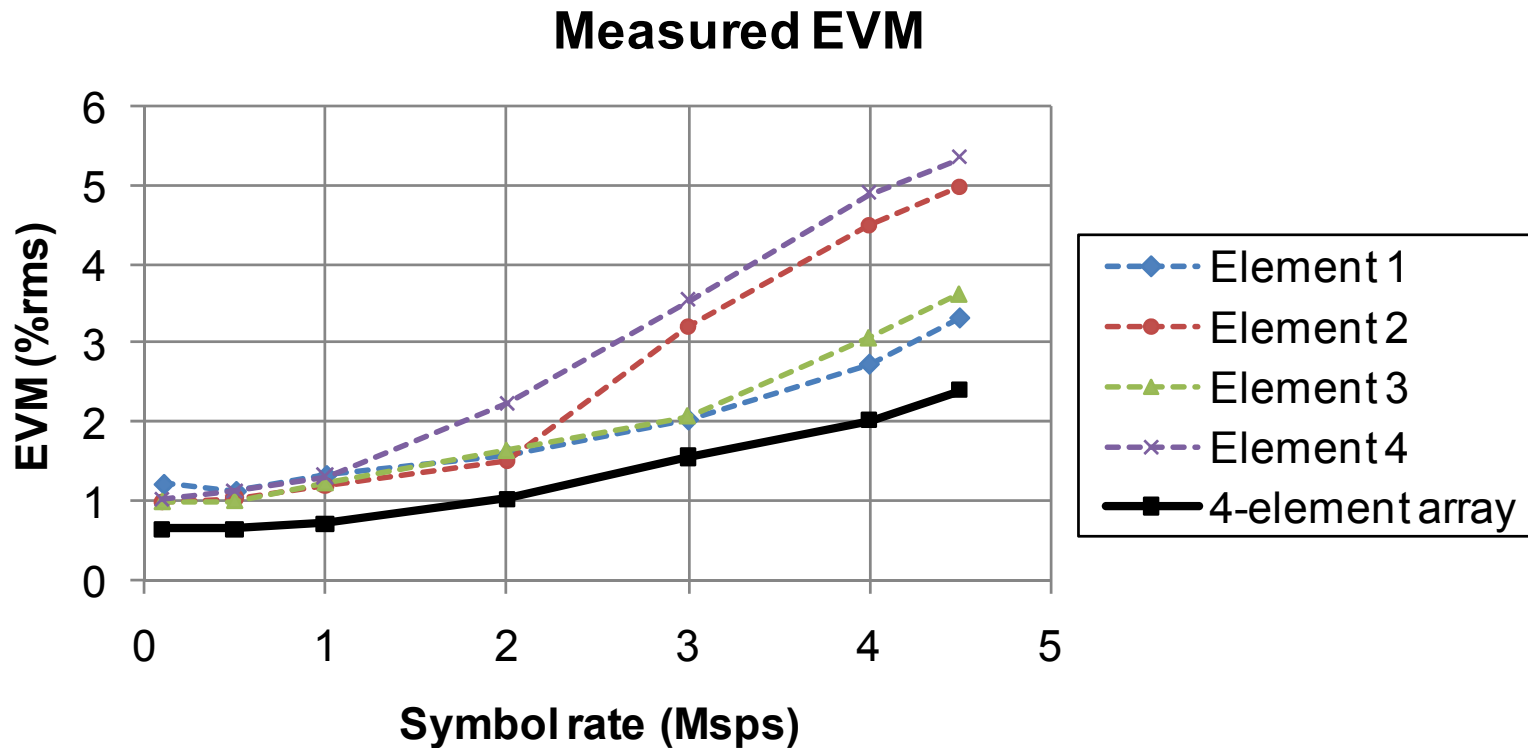
- Peak-to-null ratio $> 21.5\text{dB}$

Phase Error Calibration



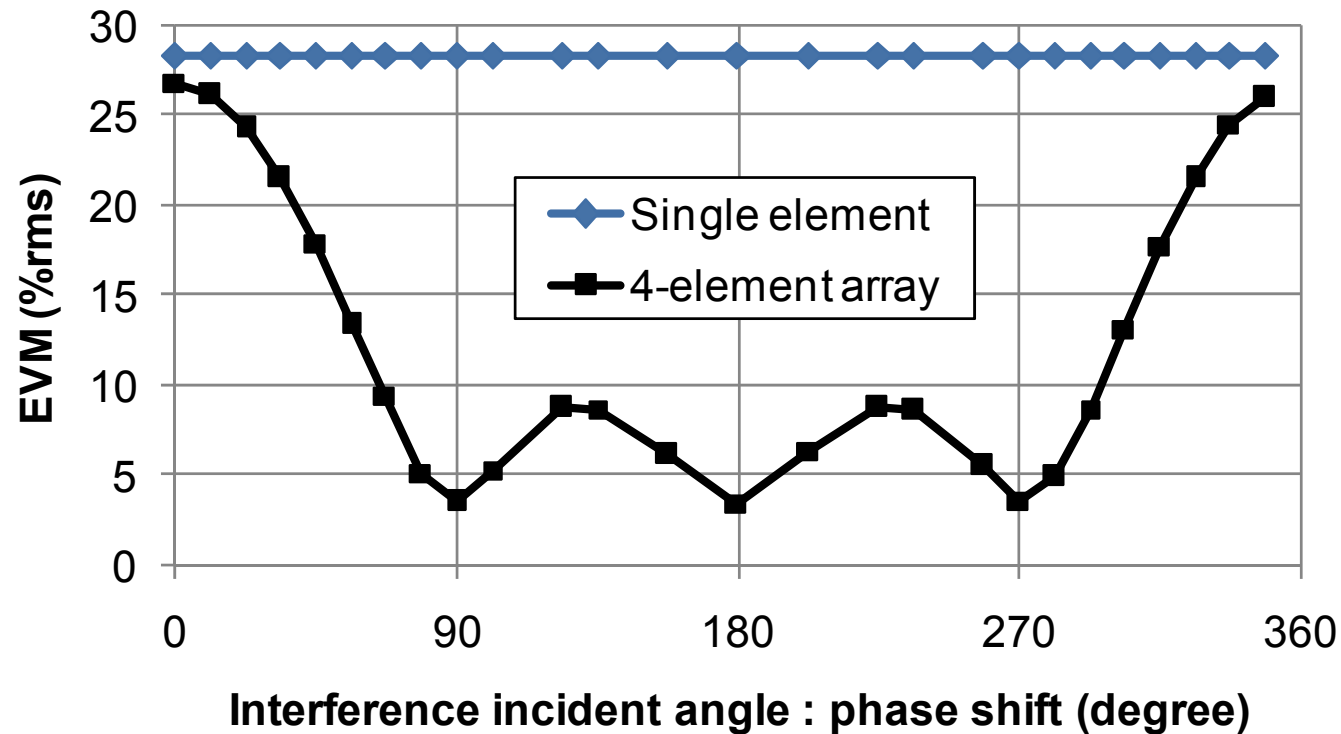
- One-time digital calibration of phase errors due to:
 - Mismatch, skews in ref signal distribution, element-by-element variation.
- On-chip phase shifting with fine resolution is essential.

Digital Modulation Performance



- Modulation format: QAM32 @ 10.4GHz carrier.
- EVM improved in array.
 - I & Q mismatch improved after signal combining.
 - SNR improved after signal combining.

Interference Rejection



- Desired signal: QPSK with 4Msps @ 10.4GHz, $P_{in} = -35\text{dBm}$, Incident angle fixed.
- Interference signal: FM with 100kHz @ 10.4GHz, $P_{in} = -45\text{dBm}$, Incident angle swept.
- Interference signal almost rejected at null positions.

Performance Summary

Receiver Element Performance

Conversion gain (6 – 18GHz)		15.7 ~ 24.7dB
Input-referred 1-dB compression (6 – 18GHz)		-25.9 ~ -14.7dBm
Input-referred IP3 (6 – 18GHz)		-17.0 ~ -5.2dBm
Input return loss (6 – 18GHz)		> 9.5dB
Cross-polarization rejection (6 – 18GHz)		> 63.4dB
Cross-band rejection (6 – 18GHz)		> 48.8dB
LO leakage (6 – 18GHz)		< -24.5dBm
Antenna-to-baseband noise figure [†] (6 – 18GHz)		2.6 ~ 3.1dB
Phase shifting resolution (6 – 18GHz)		< 5° (within 2dB amplitude variation)
RF channel spacing		225MHz (Div8 LO ₂), 300MHz (Div2 LO ₂)
Power consumption	RF and LO circuitry	658mA @2.7V, 217mA @1.6V
	Baseband buffers	328mA @1.5V
Technology		130nm CMOS
Die area		3.0×5.2 mm ²

Phased-Array Performance (4 elements measured at 6-, 10.4-, and 18-GHz)

Number of beams concurrently receivable	4
Phase shifting resolution per element	< 5°
Total phased-array gain	> 27.7dB
Beam-forming peak-to-null ratio	> 21.5dB

Conclusions

- The first tritave dual-band quad-beam phased-array receiver element in CMOS.
- RF front-end integrated from RF, LO to baseband.
- Easily scalable toward very large-scale phased arrays with low cost and high reliability.

Acknowledgments

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For additional multimedia material: See <http://www.isscc.org>

